

is characterized in that, in the counting step, the number of times pattern data is used in the test of a preset number of semiconductors is counted.

The control method of the semiconductor test apparatus of the present invention is characterized in that the storage step loads the pattern files in descending order of
 5 frequency of use based on this pattern file use frequency table after producing the pattern file use frequency table.

The control method of the semiconductor test apparatus of the present invention is characterized in that the storage step deletes the pattern in ascending order frequency of use in the case that the capacity of the executive memory is in sufficient when
 10 transferring pattern files to the executive memories.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing the structure of the semiconductor test apparatus according to an embodiment of the present invention.

15 Fig. 2 is a flowchart showing the production of the pattern file use table of the present invention, and the redistribution of the files.

Fig. 3 is a flowchart showing the transfer format of the pattern file according to the present invention.

20 Fig. 4 is a drawing for explaining the control structure of the pattern files according to a conventional example.

Fig. 5 is a flowchart showing the transfer format of the pattern files according to a conventional example.

DETAILED DESCRIPTION OF THE INVENTION

25 Below, an embodiment of the present invention will be explained referring to

the drawings. Fig. 1 is a block diagram showing the structure of the semiconductor test apparatus according to an embodiment of the present invention. In this figure, the disk apparatus 12 stores pattern files for a plurality of types of semiconductors that the control unit 10 reads in from an external memory apparatus.

5 The buffer memory 13 stores the pattern files to be used in the test of the semiconductor that are read out from the disk apparatus 12 by the control unit 10. The executive memory 17 is formed by the pattern memory 14, the MIC memory 15, and the SPG memory 16 and distributes and stores the pattern files. Here, the pattern memory 14, the MIC memory 15, and the SPG memory 16 are memories that are
10 respectively identical to the pattern memory 44, the MIC memory 45, and the SPG memory 46 in Fig. 4.

 The pattern file use frequency table storage unit 18 associates each pattern file and the number of times each pattern file is used, which is calculated by the control unit 10, and stores them.

15 In addition, the format by which the pattern files are controlled in the semiconductor test apparatus, that is, the format in which the pattern files are distributed and stored in each memory of the executive memory 17 from the disk apparatus 12, is identical to the conventional method already explained, and the explanation thereof will be omitted.

20 After the pattern files are stored, in the conventional method a test is carried out by applying the pattern data of the pattern files to the semiconductor that is the test object.

 In contrast, in the present invention, because the frequency of use for each pattern file is found, in the step of testing a preset (specified) number of semiconductors
25 that are the test objects, the frequency of use of each of the pattern files counted by the

control unit is stored for each pattern file in the pattern file use frequency table of the pattern file use frequency table storage unit 18.

This preset number represents a number of samples that will reflect the frequency of use of the pattern files among the total number of semiconductors that are the test object.

Next, an example of the operation of the embodiment will be explained referring to Fig. 1, Fig. 2, and Fig. 3.

First, referring to Fig. 2, the operation of the steps up to the point that the pattern file use frequency table has been completed and the pattern files have been optimally distributed will be explained. Fig. 2 is a flowchart showing an example of the operation of the steps up to the point that the pattern file use frequency table has been completed and the pattern files have been optimally distributed.

In step 21, the control unit 10 initializes the pattern memory 13 and each of the memories in the executive memory 17, and the pattern file use frequency table.

In addition, the control unit 10 reads out all of the pattern files to be used in the test of a semiconductor that is the test object from the disk apparatus 12, and stores the pattern files that have been read out in the buffer memory 13.

In addition, the control unit 10 distributes to each memory of the executive memory 17 the pattern files that can be accommodated in the capacity of the executive memory 17, that is, the pattern files that can be stored in the executive memory 17, read out from the buffer memory 13.

Next, in step 22, the control unit 10 carries out testing of the operation of the first semiconductor based on the pattern file of, for example, pattern 1 in the specified number of semiconductors for which the pattern file use frequency will be found.

Next, in step 23, the control unit 10 uses the use frequency of the pattern file of